the following art rejections were asserted:

- Claims 1-3, 5, 7: admitted prior art (APA)
- Claims 1-3, 5, 7: *Proc IEEE* article (Tsang *et al.*)
- Claims 6 and 11: APA or Tsang *et al.*, in the alternative

ADMITTED PRIOR ART (APA). The semiconductor device of Claim 1 (Amended) includes a second MOS transistor having the portion that is measured by fluctuation in potential. The Office Action indicates (with reference to the rejection of Claim 5) that MOS transistor 120 in the admitted prior art (APA) is the portion to be measured. However, APA FIG. 11's MOS transistor 120 and peripheral circuit 50 are distinct elements: MOS transistor 120 does not have a peripheral circuit 50. Accordingly, the APA does not disclose or suggest Claim 1.

What the APA discloses is:

> ...Therefore, when the power source potential 9 is outputted from the CMOS transistor 200, a reverse voltage is applied between the n^+ impurity region 3 and the p^- well region 6. The pn junction formed between the n^+ impurity region 3 and the p^- well region 6 is irradiated with a near-infrared laser beam 20 and intensity of a reflected light of the laser beam 20 is detected. As a result, fluctuation in potential of the n+ impurity region 3 can be observed.[1]

Thus, the APA provides a technique premised on a gate electrode 1 of MOS transistor 110 having a CMOS transistor 200, and a gate electrode 10 of MOS transistor 120 are electrically connected with each other through a wire 11.

In contrast to the APA, Claim 1 requires that the gate electrodes of the first and second transistors be electrically insulated from each other. Accordingly, even when the second MOS transistor (including a portion to be measured) is performing a switching operation, the first MOS transistor (that is part of an observation part) does not perform a switching operation.

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[1]Page 4, lines 9-15.

Thus, the structure of Claim 1 is not disclosed in or suggested by the APA, and the rejection is submitted to be improper and should be withdrawn.

Finally, Claims 6 and 7 are allowable over the admitted prior art in view of the paragraph bridging pages 3 and 4 of the Background: FIG. 11's circuit merely permits measurement of drain regions and not gate electrodes (Claim 6) or source/drain regions (Claim 7).

Thus, Claims 6-7 and 9 should be allowable by virtue of their own recitations, in addition to the features of the claims from which they directly or indirectly depend. Therefore, reconsideration and withdrawal of the rejection based on the admitted prior art (APA) are respectfully requested.

TSANG *ET AL.* Applicant also traverses the rejections based on the Tsang *et al.* article, for the following reasons.

Claim 1 (Amended) requires a second MOS transistor to have the portion that is measured. The Office Action mentions, concerning the rejection of Claim 5, that a p-channel MOS transistor (a MOS transistor connected through an output wire to an n-channel MOS transistor illuminated by a laser pulse) includes a portion to be measured (actually an output wire). However, Tsang's FIG. 18 shows that the p-channel MOS transistor does not have an output wire, and accordingly, Claim 1 is neither disclosed or suggested by the Tsang *et al.* reference.

Moreover, Tsang's FIG. 18 semiconductor device is a CMOS transistor, in which a gate electrode of an n-channel MOS transistor illuminated by a laser pulse and a gate electrode of p-channel MOS transistor are electrically connected, with a same voltage being applied to them; this contradicts the language of Claim 1 (Amended) requiring the gates to be electrically insulated from each other.

More specifically concerning Claim 6: a portion to be measured is a gate electrode of a second MOS transistor. Therefore, the semiconductor device of Claim 6 constitutes a structure in which a gate electrode and an observation part are connected by a wire, a structure that is not disclosed or suggested by the cited art.

Like the APA, Tsang *et al.* are able to indirectly confirm whether a voltage exceeding (or not exceeding) a threshold is being applied to a gate electrode, by irradiating a pn junction with a laser beam. However, *the fluctuation in potential of the gate electrode* cannot be directly measured by either the APA or Tsang *et al.* Thus, in contrast to the APA or Tsang *et al.*, Claim 6 requires that the gate electrode and the observation part are connected through a wire, and it is possible to directly measure the fluctuation in potential of the gate electrode. Accordingly, Claim 6 has a structure that is neither disclosed in or suggested by the Tsang *et al.* reference, and, accordingly has an advantage that the Tsang *et al.* arrangement cannot provide. Accordingly, the rejections of Claim 6 is submitted to be improper, and reconsideration and withdrawal thereof are respectfully requested.

For at least the foregoing reasons, Applicant submits that all active claims are allowable. Moreover, because Claim 1 is allowable, all of Claims 2-19, including those that have been officially withdrawn from consideration, should be allowable as well. Therefore, reconsideration and withdrawal of the rejections, and allowance of Claims 1-19, are respectfully requested.

In view of the present amendment and in light of the foregoing discussion, it is respectfully submitted that the case is in condition for allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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IN THE CLAIMS

Please amend claims 1, 6, and 11 as shown in the Attachment, in which underlining and bracketing show the changes introduced into the previously-pending claims to arrive at the clean claims provided below:

1. (Twice Amended) A semiconductor device, comprising:

a) a second MOS transistor, including [a second gate electrode and] a portion measured by fluctuation in potential;

b) a wire having a first end and a second end, the second end being connected with said portion measured; and

c) an observation part including a pn junction irradiated with a laser beam to detect said fluctuation in potential, wherein:

1) said observation part includes a first MOS transistor having:

i) a source/drain region including a first impurity region of a first conductivity type, that is connected with said first end of said wire and that is formed within a second impurity region of a second conductivity type; and

ii) a [first] gate electrode that is electrically insulated from [the] a [second] gate electrode of said second MOS transistor; and

2) said pn junction includes said first and second impurity regions.

6. (Twice Amended) The semiconductor device according to claim 1, wherein:

said portion measured is [a] said gate electrode of said second MOS transistor.

11. (Twice Amended) The semiconductor device according to claim 1, wherein:

a) said first conductivity type is an n type and said second conductivity type is a p type;

b) said observation part further includes:

1) a second pn junction having a p-type third impurity region connected with said wire; and an n-type fourth impurity region; and

[2) an n-type fourth impurity region; and]

c) a first fixed potential is applied to said second impurity region and a second fixed potential higher than said first fixed potential is applied to said fourth impurity region.